S.B. Roll No……..

VLSI SYSTEM DESIGN

6th/ECE/EMP/EEE/ ECEII/6188/0161/6922/May'16

Duration: 3Hrs **M.Marks=75**

SECTION A

Note: All questions in this section are compulsory.

Q1. Do as directed: **10x1.5=15**

a. VHDL stands for _____.
b. VHDL is an event-driven language. **(T/F).**
c. Identifiers are user defined words to name objects in VHDL.
d. VHDL is a concurrent language. **(T/F)**
e. Operator which calculates remainder in VHDL is _____.
f. Thigh attribute in VHDL will show _____ value in T.
g. Symbol for "not equal to" sign in VHDL is _____.
h. FPGA stands for _____.
i. Sequential system contains _____, which differentiates it from combinational system.
j. VHDL models can be of _____, _____ and _____ types.

SECTION B

Q2: Attempt any FIVE questions. **5x6=30**

a. Describe the features of VHDL.
b. What are the basic design units in VHDL?
c. What is operator overloading? Explain its use in VHDL.
d. Explain the "for" conditional statement of VHDL.
e. Differentiate between CPLDs and FPGAs?
f. How hardware description languages are different from high level computer programming languages like C++ and BASIC.
g. Write VHDL code for half adder circuit.

SECTION C

Attempt any THREE questions **3x10=30**

Q3. Explain various data types used in VHDL.
Q4. What is delay? Explain various models of delay as used in VHDL.
Q5. Design a combinational circuit of multiplexer with four input lines using VHDL.
Q6. Design a sequential circuit of 4-bit up counter with VHDL.
Q7. Write note on any **TWO**:

(a) PLAs
(b) FPAA
(c) Concurrent Statements.