S.B.	Roll	No

## DIGITAL ELECTRONICS 3<sup>RD</sup> Exam/ECE/ETV/ECEII/Comp/CSc/EEE/0620/May'17

	3 Exam/ECE/ETV/ECEII/Comp/CSc/EEE/0620/May	17	
Durat	ion: 3Hrs	M.Marks:75	
	SECTION- A		
Q1. D	o as directed:	15x1=15	
a.	The numbers of levels in a digital system are		
b.	1011 is a valid BCD number. (T/F)		
c.	Binary code of gray code 1011 <sub>gray</sub> is		
d.			
e.	The clear signal is same as reset signal.(T/F)		
f.	The fastest ADC is		
g.	The maximum count in a 4-bit ripple counter is		
h.	To convert a JK flip-flop into T flip-flop, the inputs J=K=	•	
i.	The condition S=R=1 is called ascondition.		
j.	The complement of Boolean algebra AB. (BC+AC) is	•	
k.	The radix of octal number is		
l.	The parity is used for error detection and correction. (T/F)		
m	logic family has maximum fan-out.		
n.	ASCII is acode.		
	A universal shift register can shift register left or right. (T/F)		
	SECTION- B		
Q2: A	ttempt any six questions.	6x5=30	
i.	Draw symbol and truth table of NOT, NAND and OR gate.		
ii.	Convert the following: <b>A)</b> $62_{16}$ X $36_{16}$ <b>B)</b> $341_8$ = (?) <sub>10</sub>		
iii.	Define noise margin, propagation delay and fan-out.		
iv.	Compare all logic families and their characteristics.		
٧.	Explain the operation of JK flip-flop using NAND gate.		
vi.	Explain dual slope A/D converter.		
vii.	Why universal shift registers are called universal? Explain.		
viii.	Draw and implement half adder.		
ix.	What are the applications of digital signal?		
	SECTION-C		
Atten	npt any three questions	(3x10=30)	
<b>Q3.</b> Si	mplify the given K-map and draw logic circuit using gates. F(A,B,C,D	)= ∑(0,3,6,7,9,13,14,15)	
<b>Q4.</b> Ex	plain the working of 3-bit asynchronous counter.		
<b>Q5.</b> D	raw and explain BCD to decimal decoder. Give its applications also.		
<b>Q6.</b> W	rite Short note on any two:		
(a)	4-bit adder		
(b) D/A converter			
(c) Buffer register			
(d) Latch and flip-flop			