S.B. Roll No……..

VLSI SYSTEM DESIGN

6th Exam/ECE/EMP/EEE/ECE||/6188/0161/6922/May,2015

Duration:3 hrs **Max. Marks 75**

SECTION-A

Q.1. Fill in the blanks **1.5×10=15**

1. FPGA stands for _____.
2. The keywords _____ followed by the user-defined name indicate the end of a VHDL package body.
3. The VHDL _____ data type has two possible values, true and false.
4. The _____ type declaration defines a type that has a set of user defined values consisting of identifier and character literals.
5. CPLD stands for _____.
6. VHDL is a case sensitive language. (True/False)
7. VHDL stands for_____.
8. PLA stands for _____.
9. FPAA stands for _____.
10. PEEL stands for_____.

SECTION-B

NOTE: Attempt any five questions **5×6**

1. Explain in brief the evolution of VHDL and mention the capabilities of the language.
2. Explain the different types of operators in VHDL.
3. Write down Factorial Program using loops in VHDL.
4. Explain the Inertial Delay and Transport Delay with examples.
5. Write a short note on FPGA and CPLD.
6. Write down the Program for 9-bit Parity Generator using Structural Modeling.
7. What is overloading. Explain the different types of Overloading.
8. Write a VHDL code for Full adder using Dataflow modeling.

SECTION-C

NOTE: Attempt any three questions **3×10**

1. Develop a VHDL code for 4:1 Multiplexer using Behavioral Modeling.
2. Give the classification of Data Types in VHDL. Explain Scalar Type of data with an example.
3. Explain the Function and Procedure with examples.
4. Explain the different style of modeling using VHDL taking an Example of Half Adder.
5. Explain the Following
   a. Entity b. Architecture c. Packages