S.B. Roll No.....

VLSI SYSTEM DESIGN

6th /ECE/EMP/EEE/ECEII/6188/6922/0161/Nov' 2016

Duration: 3Hrs **M. Marks: 75**

SECTION-A

Note: Attempt all questions.

Q1. Fill in the blanks: **1.5x10=15**

1. Write the difference between ROM and RAM.
2. Write down the syntax to declare entity.
3. What is CPLD?
4. Explain the significance of HDL in digital design.
5. What is overloading in VHLD.
6. What do you mean by library and package?
7. How does PLA differ from ROM.?
8. Name various concurrent statements .
9. What are various sequential statements?
10. Explain the use of WAIT statement with example.

SECTION-B

Q2: Attempt any five questions: **5x6=30**

1. What is the significance of wait statement in VHDL? Explain different types of wait statements.
2. Write a VHDL program to design 2-bit comparator circuit.
3. Explain the internal architecture of FPGA.
4. Write a data flow model for 3 to 8 decoder.
5. Write various advantages of VHDL.
6. Explain various data types in VHDL.

SECTION-C

Note: Attempt any three question: **3x10=30**

Q3. Explain behavioural, dataflow and structural modeling techniques.

Q4. Compare CPLD and FPGA in details.

Q5. Write a difference between signal and variable.

Q6. Design a BCD to gray code converter using VHDL language.