S.B. Roll No……..

**DIGITAL ELECTRONICS**

**3RD Exam/ECE/ECE-II/ETV/CSE/COMP/IT/EEE/0620/Nov'18**

**Duration: 3Hrs.** **M.Marks:75**

**SECTION-A**

**Q1. Fill in the blanks.** **15x1=15**

a. In a digital system, digital signal requires _____ channel bandwidth.
b. Collection of 4 bits is called _____.
c. Radix of octal number is _____.
d. BCD numbers express each decimal digit as a _____.
e. TTL stands for _____.
f. An inverter is also known an _____.
g. The XOR gate is sometimes referred to as _____.
h. LSI & VLSI devices use _____ technology.
i. A multiplexer changes _____data into _____ data.
j. To overcome race around condition _____type of flip flop is used.
k. A ripple counter is _____ sequential circuit.
l. IC 74194 is _____ shift register.
m. The fastest A/D Converter is _____.
n. Draw symbol of XNOR.
o. The 2's complement of 11001000 is _____.

**SECTION-B**

**Q2. Attempt any six questions.** **6x5=30**

i. Convert each binary number to decimal
   a) $(110011.11)_2$ b) $(101010.01)_2$ c) $(1000001.11)_2$
ii. Explain ASCII code and convert a binary 1001011 to gray code.
iii. What are the different error detection and correction codes?
iv. Discuss the characteristics of TTL Logic Family.
v. Explain the laws related to Boolean algebra.
vi. Explain De Morgan's theorems.
vii. Difference between Combinational and Sequential Circuit.
viii. Design 4 bit ring counter.

**SECTION-C**

**Note: Attempt any three questions.** **3x10=30**

**Q3.** Explain the universal property of NAND & NOR Gate.

**Q4**. Draw the Karnaugh Map for the following of four variables

i. F(A,B,C,D)=∑m(0,1,2,3,4,5,10,11)
ii. F(A,B,C,D)=∑m(2,3,6,7,10,11,14,15)

**Q5.** Write a short note on the following. **(any two)**

a) Half Adder b) DEMUX c) Dual slope A/D Converter.

**Q6.** Explain the working principle of JK Master/ Slave flip flop and its truth table.

**Q7.** Explain Serial to Parallel Shift Register.